# A Mixed Signal Adaptive Ripple Cancellation Technique for Integrated Buck Converters

by

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A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved November 2016 by the
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December 2016

# ABSTRACT

Switching regulator has several advantages over linear regulator, but the drawback of switching regulator is ripple voltage on output. Previously people use Low Drop-Out regulator(LDO) following a buck converter and multi-phase buck converter to reduce the output ripple voltage. However, these two solutions also have drawbacks and limitations.

In this thesis, a novel mixed signal adaptive ripple cancellation technique is presented. The idea is to generate an artificial ripple current with the same amplitude as inductor current ripple but opposite phase that has high linearity tracking behavior in terms of amplitude and phase. To generate the artificial triangular current, duty cycle and amplitude information is needed. By sensing the SW node, the duty cycle can be obtained; by using feedback the amplitude of the artificial current can be regulated. The artificial ripple current cancels out the inductor current, and there will result in a very low ripple output current flowing to load. In top level simulation, 19.3dB ripple rejection can be achieved. And this technique has much less power dissipation than any other solution with linear regulator.

ACKNOWLEDGMENTS

First of all, I want to express my sincere gratitude to my thesis advisor and committee chair, Professor Bertan Bakkaloglu, for advising this challenging project.

I am also grateful to Professor Jae-sun Seo and Professor Qin Lei for being committee members of my thesis.

Ming Sun, Kishan Joshi, Debashis Mandal, Raveesh Magod, Shricant Singh and Navankur Beohar gave me help and support during the project. I thank all.

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Chapter 1

# INTRODUCTION

## 1.1 Ripple Analysis of DC-DC Switching Regulator

DC-DC switching regulators, where power transistors are operated in switching mode instead of linear mode, are widely used in electronic devices powered by batteries nowadays. For switching-mode regulator, when the power transistor is on and conducting current, the voltage drop across it is minimal. When the power transistor is off and blocking high voltage, there is almost no current through its power path. So the semiconductor transistor is like an ideal switch and power loss is very small, as is shown in figure 1.1 [7] [11].

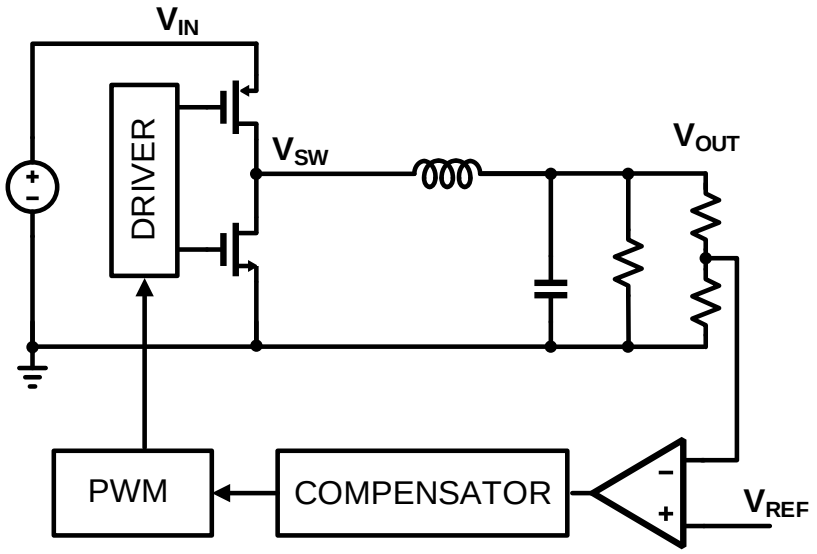


Figure 1.1: System Diagram of Buck Converter.

Switching regulators have three main advantages over linear electronics approach (e.g. Low Drop-Out Regulator )

1) Switching converters can efficiently generate regulated supply voltages which are

higher than battery supply voltage (e.g. Boost or Buck-Boost converter), which is very useful when battery voltage drops to the level lower than the required regulated voltage as stored energy is drained. This step-up function can never be realized by linear approach.

2) Switching regulators have inherent advantage on power efficiency over linear approaches. Since input current is always equal to output current for LDO, the efficiency can be calculated easily as Efficiency=$V_{OUT}/V_{IN}$. For some common use in portable system, $V_{BAT}$=4.2V, $V_{REG}$=1V, then

$$Efficiency(\%) = \frac{V_{\text{REG}}}{V_{\text{BAT}}} = \frac{1}{4.2} = 21\%$$

While for switching regulators the efficiency can reach 80%-90% in all application situations. Low power dissipation and high power density in quite small size also are reasons to use switching regulator instead of linear regulators or LDOs.

3) Switching regulators can help make isolated power supply system more compact and less costly than the linear approach counterpart. The transformer, LC filter can be much smaller with switching regulator. While it is quite difficult to realize with LDOs.

However, the disadvantage of switching regulator is its output voltage ripple due to switching operation.

In recent decades, more and more devices are integrated onto single chip, and the chip function is becoming more and more complicated. The demand with good power quality, (i.e low voltage ripple and low noise) has been increased remarkably. Switching-mode regulator's drawbacks are output voltage ripples and switching noises. For portable device, inductor with smaller size is preferred in order to make PCB more compact and system cost lower. Smaller inductance results in larger current ripple at the output of regulator in steady-state operation.

The ripple voltage has two contributors: one is output capacitor, the other one is ESR of that cap.

1) $C_{OUT}$

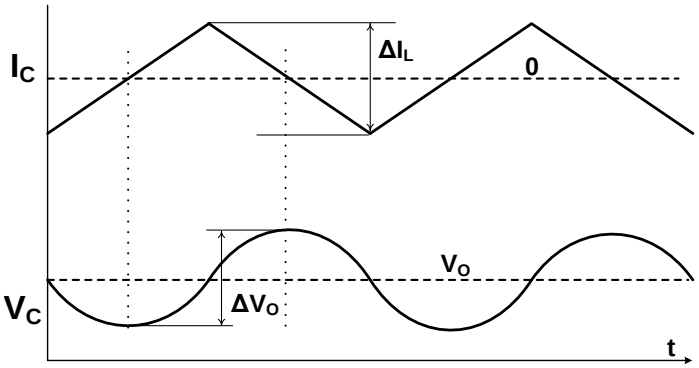


Figure 1.2: Ripple voltage on output capacitor of Buck.

With ideal capacitor, when inductor current is higher than DC load current, the output capacitor gets charged and voltage on it starts to rise. When inductor current is lower than DC load current, the voltage on output capacitor starts to drop.The ripple voltage is dependent on capacitance value, inductor current ripple and switching frequency.

$$\Delta V_O = \frac{\Delta Q}{C} = \frac{1}{2} \cdot \frac{\Delta I_L}{2} \cdot \frac{T_S}{2} \cdot \frac{1}{C} = \frac{1}{8} \cdot \frac{\Delta I_L \cdot T_S}{C}$$

2) ESR of $C_{OUT}$

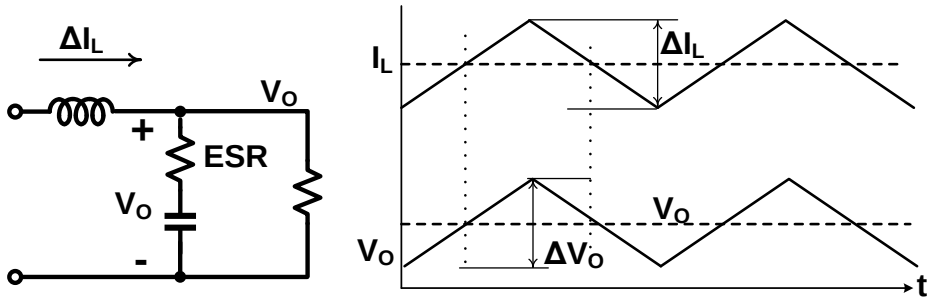


Figure 1.3: Ripple voltage due to ESR of $C_{OUT}$.

Presence of capacitor ESR (equivalent series resistance) significantly changes the capacitor ripple voltage magnitude and wave shape.

$$\Delta V_{O,ESR} = \Delta I_L \cdot R_{ESR}$$

If the voltage ripple is large, there will be several disadvantages.

1) Large ripple degrades component reliability and longevity. Most capacitors have certain tolerances for voltage ripple. Exceeding the rated levels of ripple for a capacitor can lead to stability concerns. The ripple current heats the capacitor, and too much temperature rise will cause the capacitor to exceed its maximum permitted core temperature and fail quickly [6].

2) For digital systems powered by DC-DC converter, one significant challenge is minimizing clock jitter while meeting the hardware design's functional requirements. The ripple on the regulator directly impacts the jitter performance of digital system. Achieving the lowest clocking jitter requires high-performance of the power regulator.

3) For other high-performance mixed-signal system (such as data converter) and RF amplifiers, the ripple on the power supply also has negative impact. Clocking jitter induced by bad power supply degrades Signal-to-Noise Ratio(SNR) of Analog-to-Digital Converter(ADC); For RF amplifier, additional spectral leakage comes from noise or voltage ripple on the power supply.

## 1.2 Prior Work Limitation

To obtain better power quality, there are two existing solutions.

1) A common way is cascading a LDO with a DC-DC converter,as is shown in figure 2.1. The switching regulator provides higher efficiency and the linear regulator provides lower noise. [16] [12] But this solution has drawbacks, high power consumption and PSRR bandwidth limitation of LDO.

2) Multi-phase dc-dc converter is another way to reduce ripple, as is shown in figure 2.4. For ideal two-phase buck converter, the output voltage ripple is zero at exact 50% duty cycle. For ideal four-phase buck converter, the output voltage ripple is zero at exact 25%,

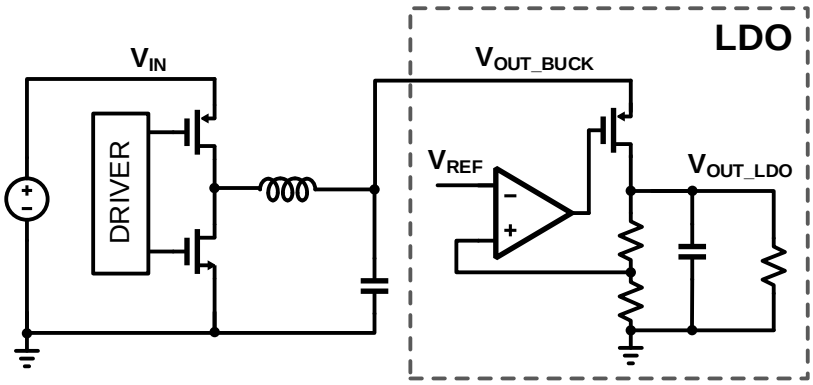


Figure 1.4: Buck converter followed by LDO.

50%, 75% duty cycle. The ripple voltage may be still quite large at some arbitrary duty cycle. Detailed analysis of these two existing solutions is discussed in Chapter 2.

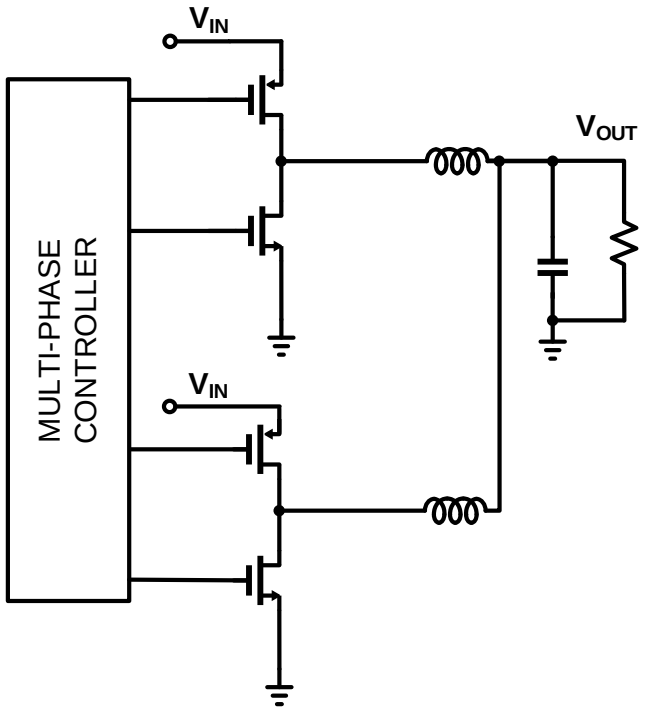


Figure 1.5: Buck converter with multiphase.

Besides, there are some other techniques to cancel the inductor current ripple [10]. But obvious disadvantages can be found. First, on-chip inductor is needed; Second, AC mismatches in amplitude, delay will limit the cancellation accuracy.

## 1.3 Highlight of This Works Contribution

A Mixed-signal adaptive ripple cancellation technique is proposed to generate an inverse current waveform of the inductor current that has high linearity tracking behavior in terms of amplitude and phase, as is shown in figure 1.6. To generate the artificial triangular current, duty cycle and amplitude information is needed. By sensing the SW node, the duty cycle can be obtained; by using feedback the amplitude of the artificial current can be regulated. In other words, the AC portion of bucks inductor current is reproduced. Subtracting the artificial current from the inductor current will result in a zero-ripple output current flowing to load.

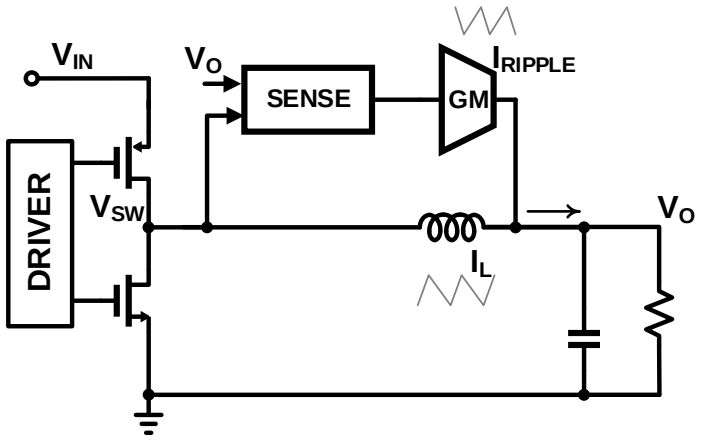


Figure 1.6: Proposed Ripple Cancellation Technique.

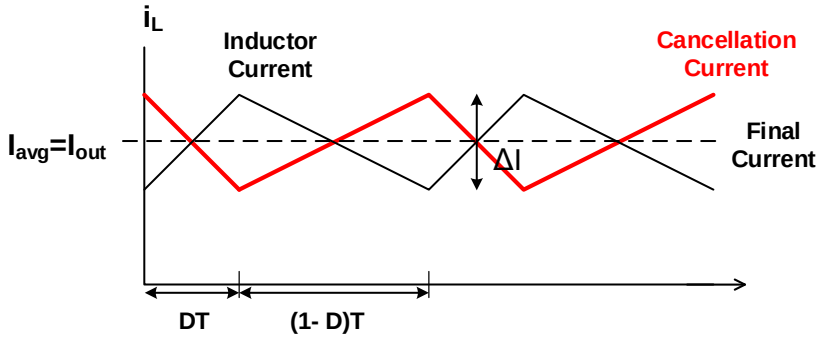


Figure 1.7: Waveform of ripple cancellation.

In figure 1.7 , the black line is original inductor current of buck; the red line is artificial ripple current generated by this proposed canceller. Detailed circuit structure and block diagram is presented in Chapter 3.

## 1.4 Thesis Organization

The thesis is organized in five chapters:

Chapter 1 gives an introduction of this work.

Chapter 2 presents prior work on ripple reduction technique.

Chapter 3 covers the adaptive ripple cancellation technique from system structure to each individual block.

In Chapter 4, top level simulation result and the chips layout concern are presented.

In Chapter 5, conclusion summary and future improvement are discussed.

Chapter 2

# PRIOR WORK OF RIPPLE REDUCTION

As is known to all, function of single IC chip gets more complicated and the requirement for power quality becomes higher. Switch-mode regulator is preferred, but its output voltage ripple needs to be suppressed. There are two existing popular solutions, which will be discussed below.

## 2.1 Buck Converter Followed by LDO

High quality Low noise power supplies is required in application of high speed communication or signal processing. A buck converter followed by a linear regulator is a popular solution, which has obvious advantages.

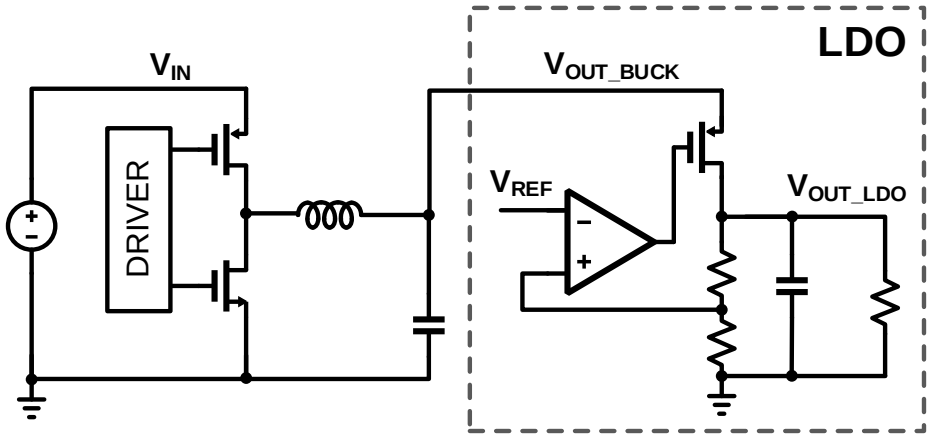


Figure 2.1: Buck converter followed by LDO.

1) Compared with LDO alone solution, buck followed by LDO provides much higher efficiency. $V_{BAT}$=4.2V, $V_{REG}$=1V, then

$$Efficiency(\%) = \frac{V_{\text{REG}}}{V_{\text{BAT}}} = \frac{1}{4.2} = 21\%$$

2) Compared with Buck converter alone solution, buck followed by LDO provides better ripple voltage rejection. LDO provides shielding function from fluctuation in power supply rails, as is known as Power Supply Rejection (PSR, which is equivalent to the term PSRR in LDO application area).

$$PSR = 20 \cdot log10(\frac{V_{\text{RIPPLE,OUT}}}{V_{\text{RIPPLE,IN}}})$$

In a simple form, the PSR transfer function can be regarded as the effect of a voltage divider caused by the impedance between supply and LDO output and the impedance between LDO output and ground, as is shown in figure 2.3.

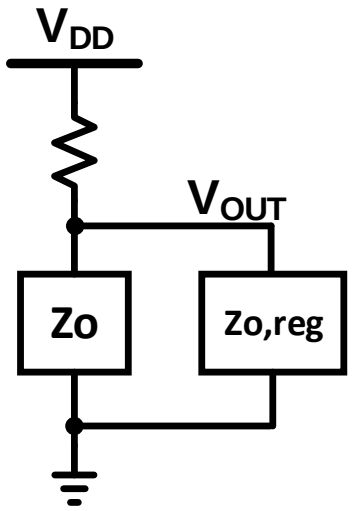


Figure 2.2: Intuitive model for PSR performance of LDO.

$$PSR = \frac{V_{\text{OUT}}}{V_{\text{DD}}} = \frac{Zo//Zo,reg}{rds + (Zo//Zo,reg)}$$

This is an intuitive model for analyzing the PSR of a typical linear regulator. This

model consists of an impedance ladder comprising of the channel resistance of the pass device (rds), and a parallel combination of the open-loop output resistance to ground (Zo), and the shunting effect of the feedback loop (zo-reg), where Zo is a function of feedback resistor divider, output capacitor and its ESR, and if we suppose $A_{OL}$ is open loop gain and $\beta$ is the feedback divider's ratio,

$$Zo, reg = \frac{Zo//rds}{A_{OL} \cdot \beta}$$

Since Zo and Zo-reg are frequency dependent, the PSR performance varies over a large range of frequency [9], as is shown in fig 2.3.

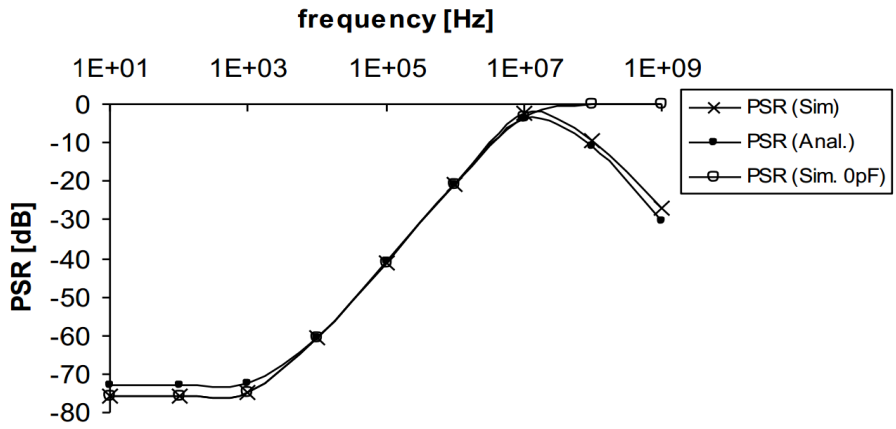


Figure 2.3: PSR performance of LDO.

A LDO following buck converter does help reject voltage ripple, but there are 2 main disadvantages.

1) As shown in the fig above, the PSR usually deteriorates as frequency goes higher. At low frequency, the high loop gain of LDO plays an important role in achieving good PSR. At moderate frequency, the amplifiers bandwidth limitation effect deteriorate PSR of LDO. At high frequency, the output capacitor shorts LDO output to ground (but ESR of the cap is still there), which causes an improvement in PSR. Most of buck converters work at

frequency near 1 MHz, and the voltage ripple on buck output is nearly 1MHz. At the same time, the PSR at 1MHz is less than 20dB, which does not offer very good performance.

2) The power consumption is quite large. If the voltage difference between LDO input and output is small or the LDO operates in dropout, the PSR will deteriorate to a point where the ripple noise at the input directly goes to the output. Therefore the voltage difference between the LDO input and output is usually larger than 300mV. For most portable devices, 300mV is a quite large value. From another aspect,the battery voltage of nowadays' portable devices is usually 4.2V, and the digital systems usually work at 0.8V. For 500mA load condition, the power dissipation at pass device is quite large,

$$P_{LOSS} = (4.2 - 0.8) \cdot (0.5) = 6.8W$$

3) Another output capacitor is needed for LDO's output, which increases the system cost and PCB area.

## 2.2 Multiphase DC-DC Converter

Another suitable approach to reducing output voltage ripple is to use a multiphase buck controller [1] [2]. Figure 2.4 shows a two-phase circuit.

It is clear that the phases are interleaved. Interleaving reduces ripple currents at the input and output. For a well-designed 2-phase buck converter, in ideal situation the output ripple voltage is zero at 50% duty cycle; the output ripple voltage also gets reduced at other duty cycle [4] as is shown in figure 2.5. For a well-designed 4-phase converter, the output ripple voltage is zero at 25%, 50%, 75% duty cycle.

However, there some drawbacks of multiphase buck converter in the use of reducing output voltage ripple.

1) For different duty cycle, the ripple reducing amplitude is different. If the DC-DC

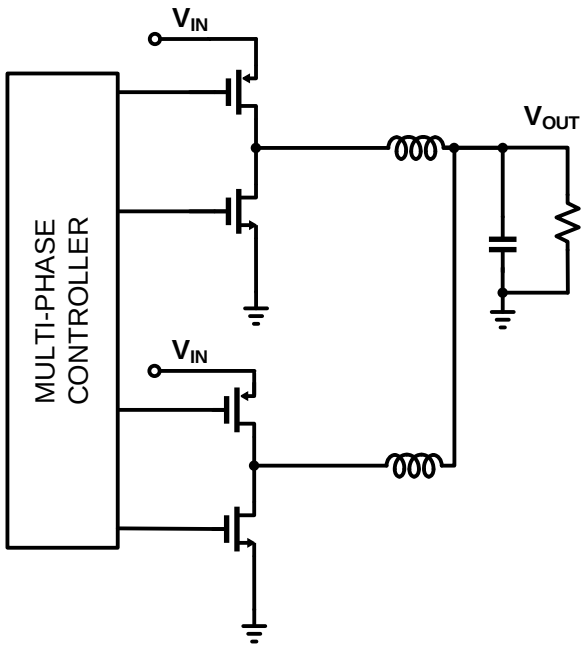


Figure 2.4: Buck converter with multiphase.

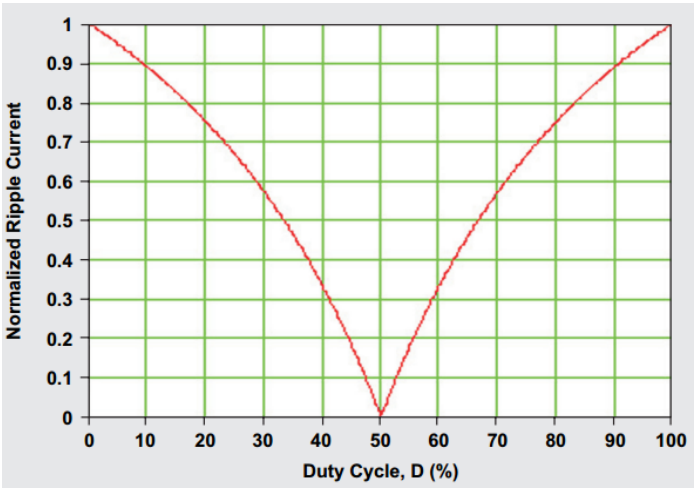


Figure 2.5: Normalized ripple of two-phase buck converter.

converter is often used in 10% or 90% duty cycle, then the ripple reducing effect is very tiny.

2) More than one inductors are needed, which increases the system cost, PCB design complexity and its area.

3) The design complexity of multiphase buck is far beyond single phase one. For phase interleaving, a PLL/DLL and some control mechanism are usually needed to guarantee correct phases are locked; inductor currents balancing between phases also needs to be taken care of. In addition to the design complexity, the bigger chip die size increase the total cost.

Therefore, both of the prior works have serious weakness and drawbacks.

# Chapter 3

# MIXED SIGNAL ADAPTIVE RIPPLE CANCELLATION TECHNIQUE

For high performance system, the requirement for high-quality power supply is becoming higher and higher. Although previous solutions, buck converter followed by a LDO and multiphase buck, have some effect on ripple voltage reduction, the limitation and disadvantages of these approaches are apparent.

A new mixed-signal adaptive ripple cancellation technique is proposed which generates an artificial ripple current with inversed phase to cancel inductor ripple current. This new approach has three main advantages:

1) It has better ripple suppression performance than the previous approach. It provides as high as 20dB ripple rejection ratio at any duty cycle.

2) It consumes much less power than LDO or buck converter followed by LDO structure.

3) It is quite flexible in application. One way is to integrate the canceller with buck on the same chip, the other way is to put the canceller on a different chip. The latter one is even more useful. No matter what buck converter is given, by putting the canceller chip on the board, low ripple and high-quality power supply can always be achieved.

## 3.1 Power Dissipation Comparison with LDO

First of all, the power dissipation of proposed canceller is a matter of concern. A power dissipation comparison is made between LDO and proposed canceller.

For example, if LDO has 1A DC current load, as is shown in figure 3.1, the 1A DC current flows through the pass device, which is a large amount of power.

On the other hand, if buck converter with ripple canceller also has 1A DC current load, as is shown if figure 3.2, the DC and AC current are flowing through inductor, only an AC current flowing through the canceller's transconductance (GM) stage, about 350mA$_{PP}$. Thus from this brief analysis, a conclusion can be made that buck converter with ripple canceller has much less power loss.

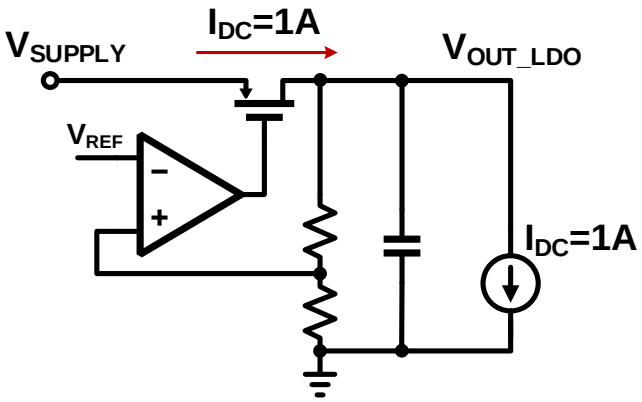


Figure 3.1: Power dissipation of LDO's pass device.

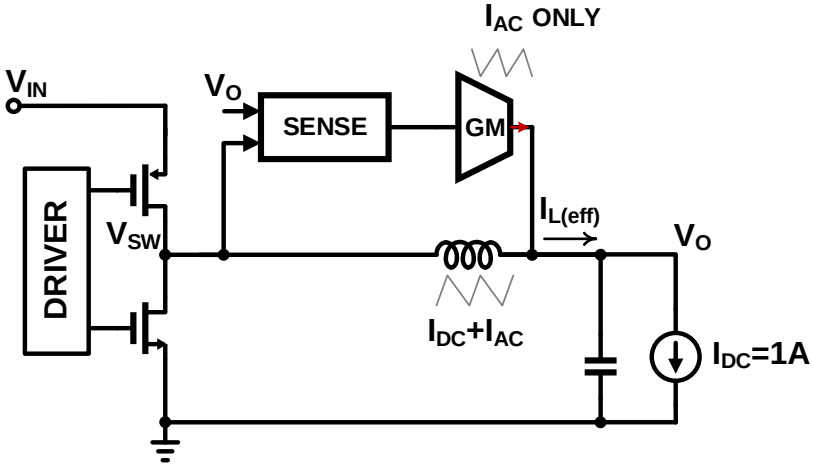


Figure 3.2: Power dissipation of proposed canceller.

## 3.2 System Structure

The system structure is shown below in fig 3.3, which includes four main parts: duty cycle sensing part, artificial ripple magnitude control part, an artificial ripple current generator, and a phase lock loop (PLL).

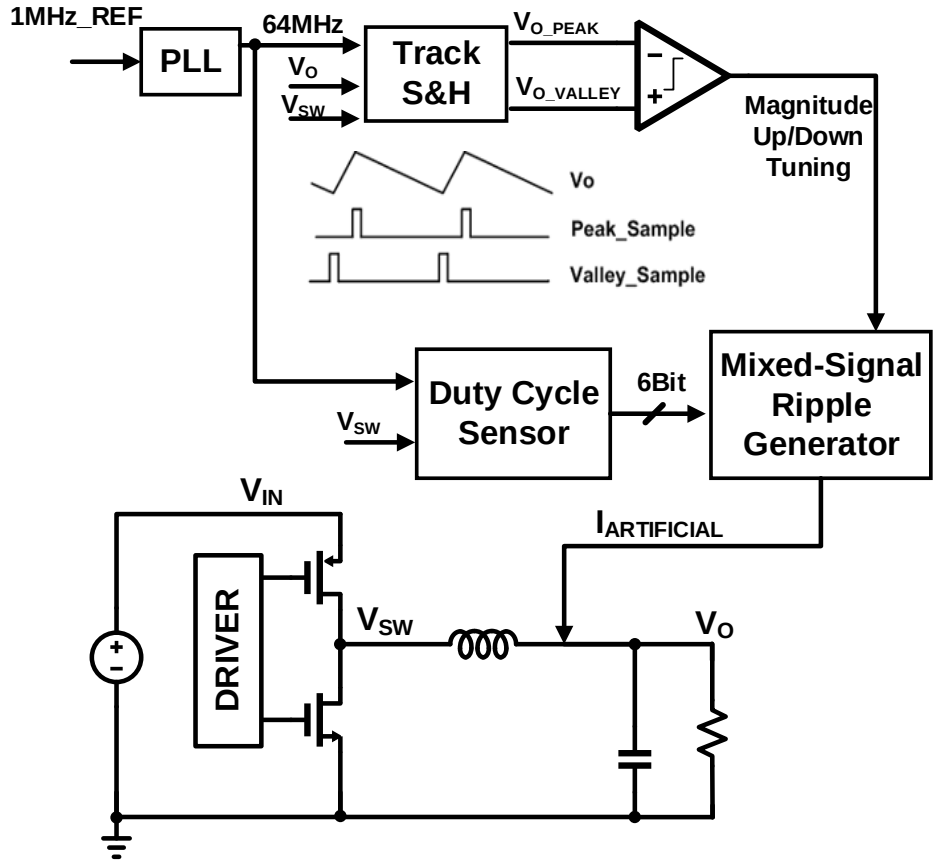


Figure 3.3: System structure of this work.

a) The duty cycle sensing block converts duty cycle information from on interval of SW node to 6 bits digital signal, and gives indication to make artificial ripple synchronized with original buck's inductor current.

b) The artificial ripple magnitude controller samples the peak and valley value of buck's output voltage and compares these two values by using a high-speed low-offset comparator. The comparator outputs 1 bit Down signal. If the valley is lower than the peak, the

magnitude of generated ripple will gets larger; if the peak is not higher than the valley, the magnitude of the generated ripple will turn smaller.

c) The ripple current generator, as is shown in figure 3.4 receives the signals from the duty cycle sensing block and the artificial ripple magnitude controller and generates a triangular voltage signal on a capacitor. After removing the DC portion, the triangular voltage is sent to a high power GM stage to generate the ripple current.

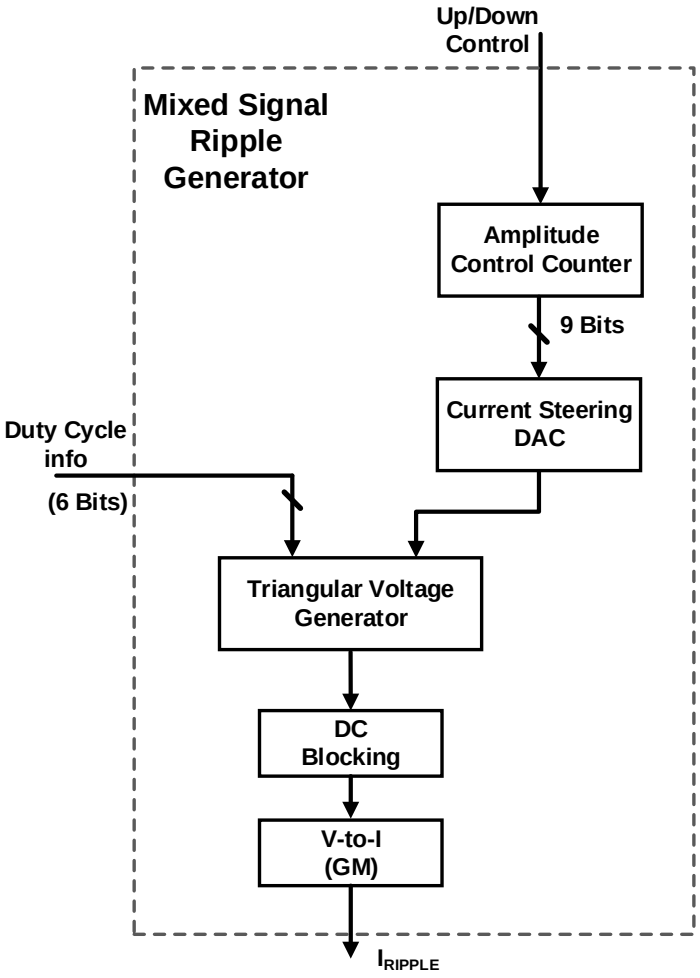


Figure 3.4: Diagram of mix-signal ripple generator.

d) The PLL generates a low noise 64MHz clock by using a 1MHz reference clock signal or SW switching signal. The 64MHz clock is used in duty cycle sensing block and output voltage peak and valley sampling block.

## 3.3 Duty Cycle Sensing

The duty cycle sensing block is functioning as a TDC (Time to Digital Converter) to measure buck converter's on time interval.The schematic is shown in figure 3.5. The lower part is 4 bits pre-distortion tuning control, which helps manually add offset on the output bits if SW signal gets distorted during the transmission.

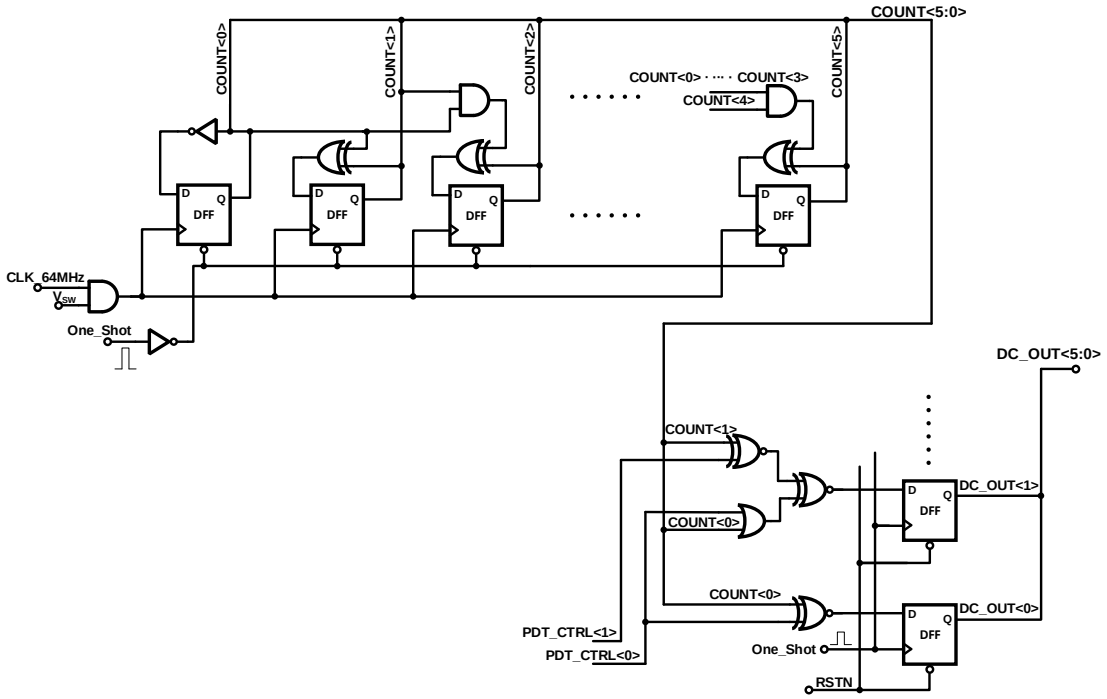


Figure 3.5: Schematic of duty cycle sensor and pre-distort tuning.

The measurement bases on the low-noise 64MHz clock from PLL. When SW node rises to high level the counter starts counting clock signals and terminates counting after SW node goes low, as is shown in figure 3.6.

The time interval $T_{ON}$ between start and stop is then

$$T_{ON} = n \cdot T_0$$

where $T_0$=1/$f_0$=15.6ns, which is the period of the reference clock; and n, the number of

counts in 6-bit binary code format can be obtained. In the waveform, the first waveform is SW, the on-interval is 200ns and switching frequency is 1MHz. The second waveform is SW & 64M clock signal, which is several consecutive pulses. The third one is 6-bit output signal of this block which counts the number of the pulses, it is 001101 which is 13 in decimal format pattern.

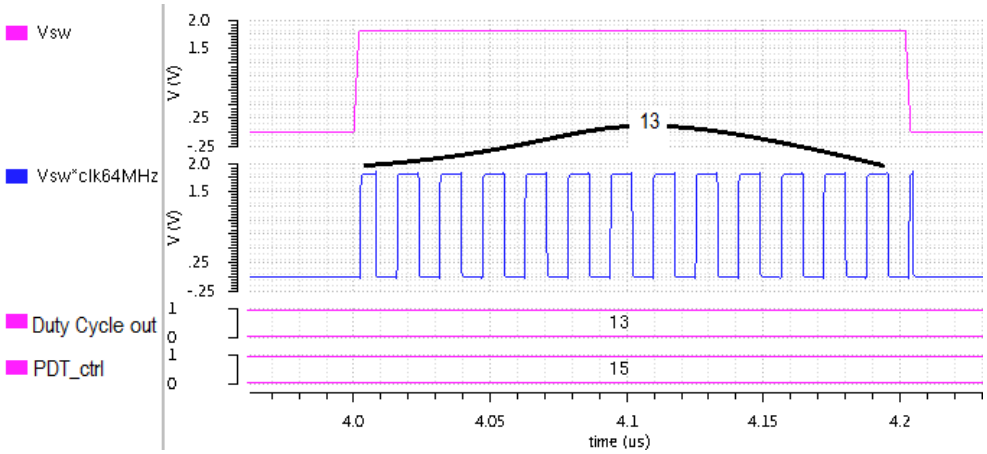


Figure 3.6: Waveform of Duty Cycle Sensor.

Lets verify the duty cycle sensor. For 6-bit binary format code, the full-scale range is 63. Then 13/63 is very close to 20%, which means the duty cycle translation is successful. The 6-bit code will be delivered to triangular voltage generator in ripple current generator.

Figure 3.7 indicates the pre-distortion tuning function. At default setting, the 4-bit pre-distortion control is 15 (1111 in binary format), and duty cycle senor output is 13; when pre-distortion control minus 1 to 14, duty cycle sensor output also minus 1 to 12. Thus if SW signal gets distorted during the transmission, some offset can be added manually.

## 3.4 Artificial Ripple Amplitude Control

Next important unit is artificial ripple magnitude control part shown in figure 3.8. It includes a triangular voltage generator, a DC blocking cell and a power transconductance GM stage. The triangular voltage generator works like a charge pump, by tuning the sourcing

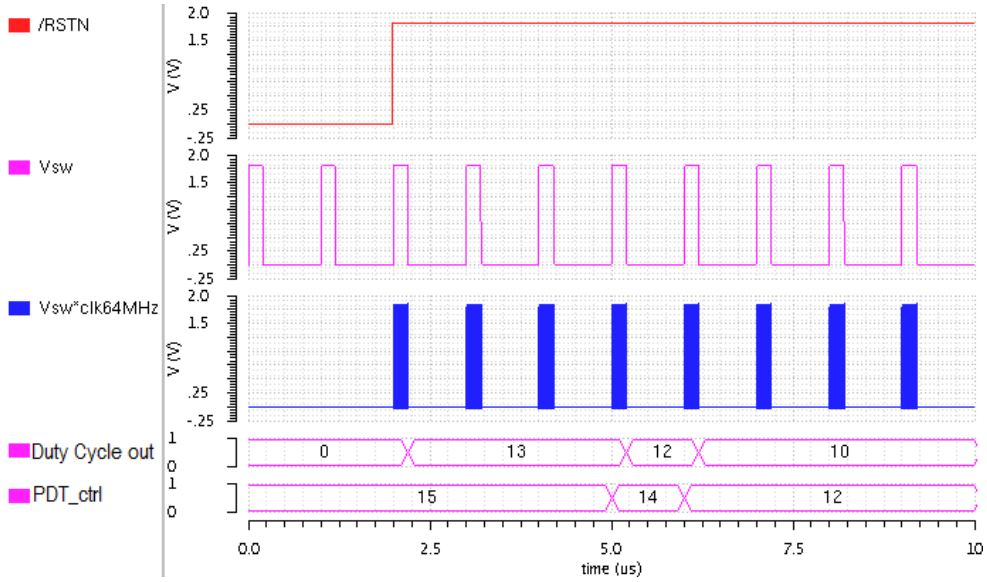


Figure 3.7: Pre-distort Tuning of Duty Cycle Sensor.

current and sinking current, the amplitude of peak-to-peak voltage on Cap gets modified. The Up/Down signal coming from SW node controls the switches to determine the cap voltage to rise or to fall. The DC blocking circuit and power transconductance stage convert the triangular voltage to the artificial ripple current. Each sub-block will be introduced next.

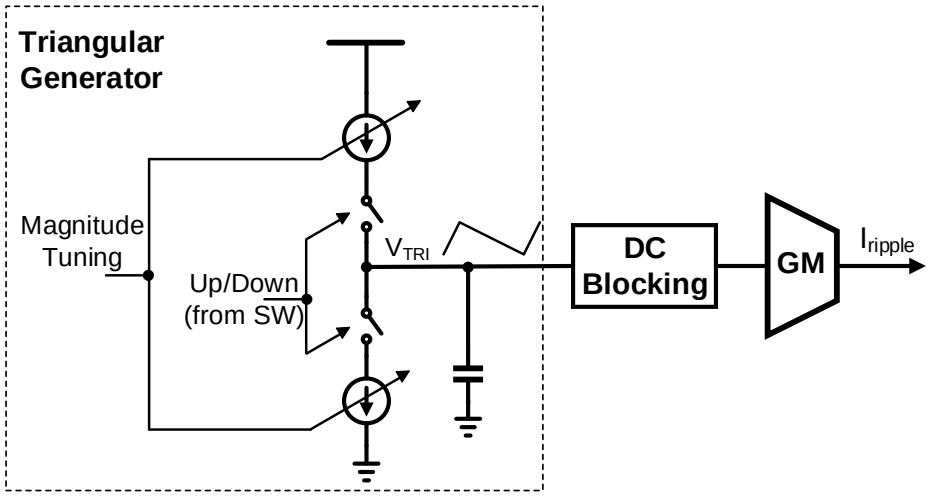


Figure 3.8: Artificial Ripple Current Generator.

1) Peak/Valley Pulse Generator

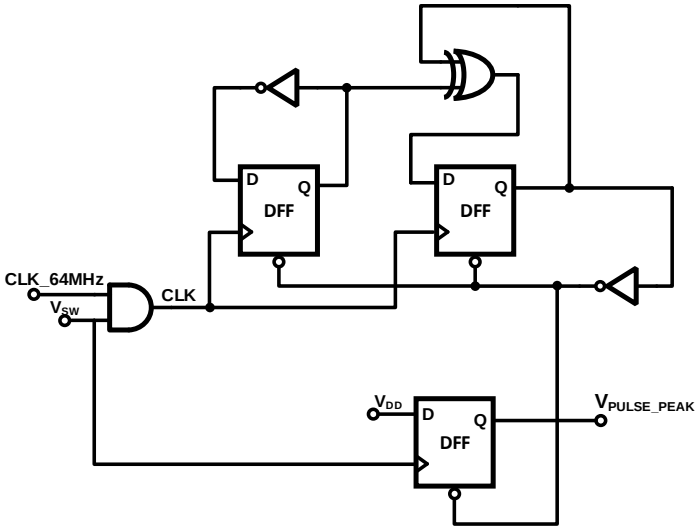


Figure 3.9: Schematic of Peak/Valley Pulse Generator.

Because the ESR dominates the Buck output ripple, the output voltage ripple and inductor current ripple are in the same phase. One pulse at SW rising edge is generated to sample $V_{OUT\_VALLEY}$, and another pulse at SW falling edge to sample $V_{OUT\_PEAK}$. Thus, the peak and valley of buck output ripple voltage can be sampled accurately.

The schematic of peak/valley pulse generator is shown below. The schematic is shown in figure 3.9.

It generates two 25ns pulse at rising and falling edge of SW node, whose waveform is shown in figure 3.10.

2) Sample/hold & Comparator

By using peak and valley time-pulse and two switch-cap amplifiers, the peak and valley values of buck output ripple are sampled and refreshed every clock period, as shown in figure 3.11. Non-overlapping clock signals are generated for bottom plate sampling, thus signal-dependent charge injection can be minimized. Take the peak value sampler for

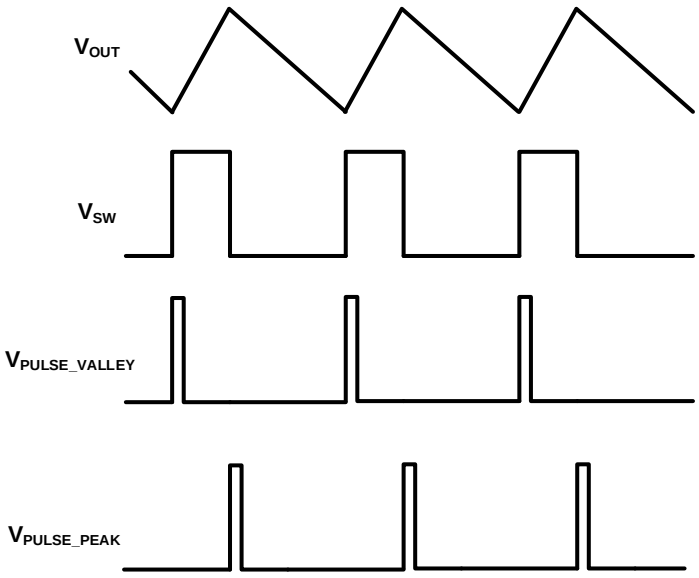


Figure 3.10: Waveform of peak/valley pulse generation.

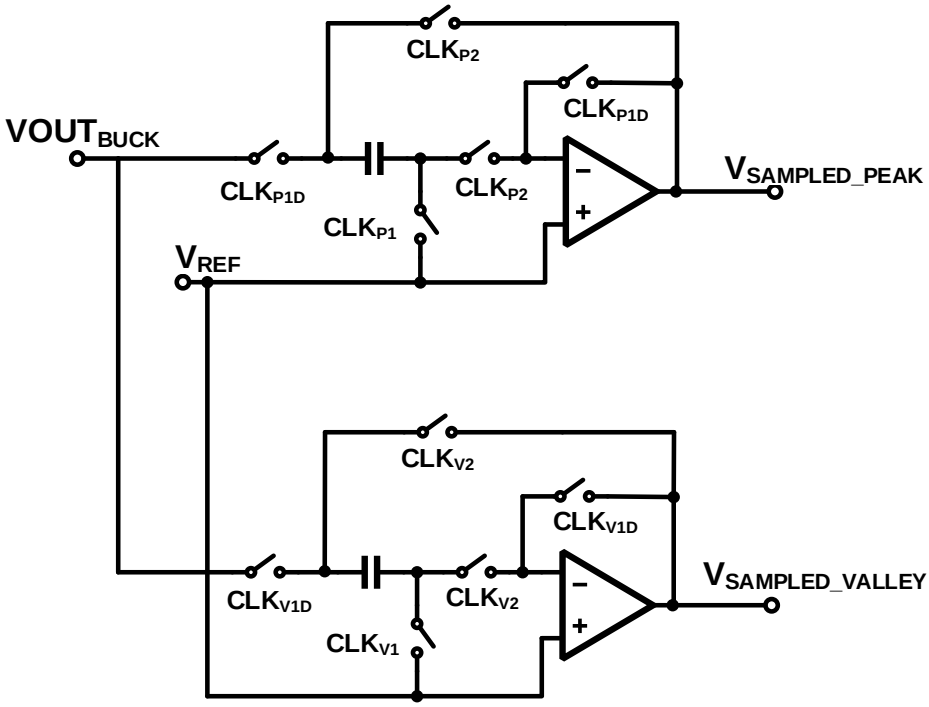


Figure 3.11: Schematic of peak/Valley sample and hold.

example, CLK_P1 phase is the sampling phase, CLK_P2 phase is the output phase [17].

The peak and valley values of buck output ripple then are fed into the high-speed com-

parator, which contains a pre-amplifier and a latch comparator. The comparator is needed to compare whether peak voltage is much greater than valley voltage. In order to get the propagation time of the comparator as small as possible, 3-stage wide-bandwidth amplifier, in fig 3.12, [3], [15], [8] is used to enlarge the input difference to a sufficient large value and apply it to a latch. The regenerative latch comparator uses positive feedback to expedite the comparison of two signals, as is shown in figure 3.13.

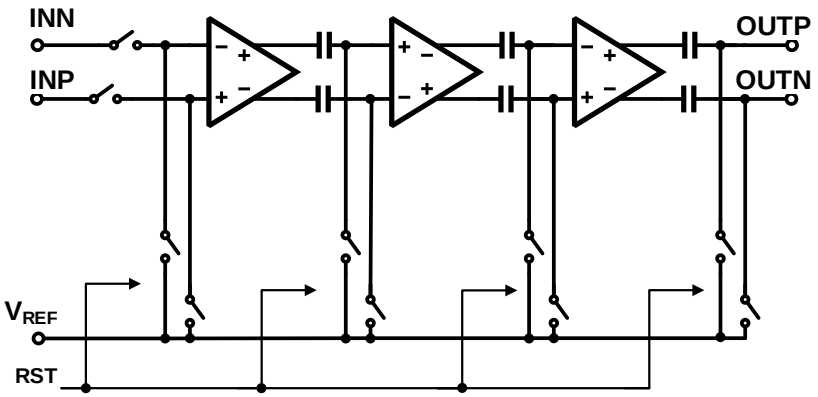


Figure 3.12: Schematic of preamplifier.

A D flip-flop is placed after the latch comparator. The output of the D flip-flop indicates whether the peak value of the buck output ripple voltage is higher than the valley value. If DOWN signal is high, the peak value is higher than the valley value, and larger amplitude artificial current ripple with inverted phase is required; If DOWN signal is low, the peak value is very close to the valley value, and smaller amplitude artificial current ripple with inverted phase is required. Therefore, after the ripple cancellation system settling down, the DOWN signal should toggle from VDD to GND continuously, as is shown in figure 3.14.

The down signal is then fed into an amplitude control counter (figure 3.15), and 9 bits digital signal comes out of the counter. The amplitude control counter is just a digital low pass filter or accumulator.

3) Current-steering DAC

Followed by the digital low-pass filter is a 9-bit current-steering Digital-to-analog con-

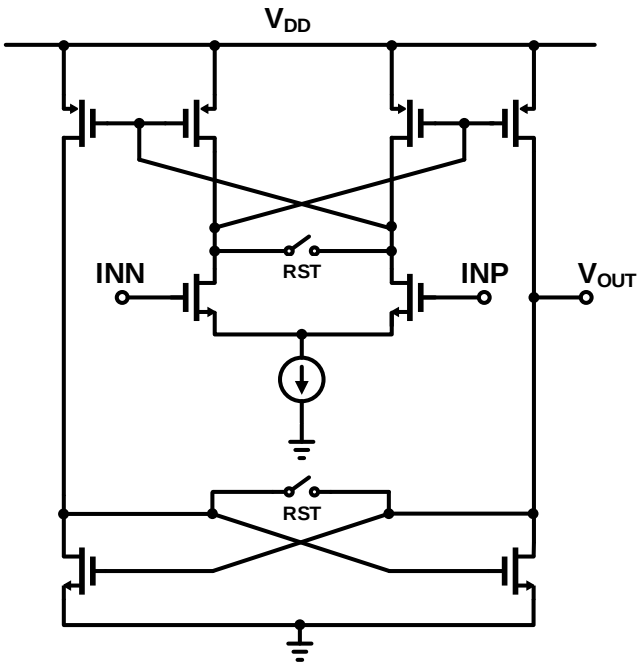


Figure 3.13: Schematic of latch comparator.

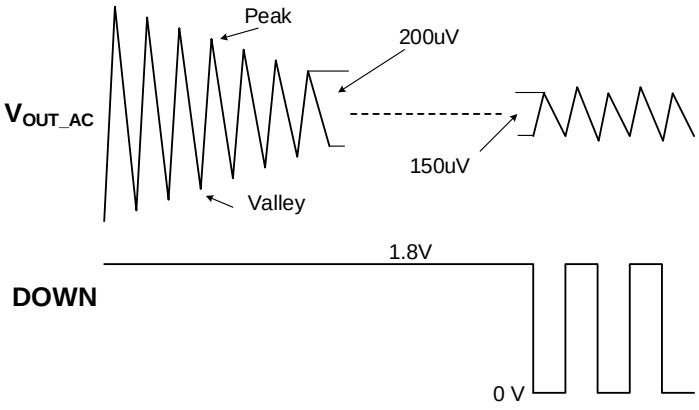


Figure 3.14: Waveform of peak/valley comparator.

verter (DAC), which will transform the digital code into the current domain to tune the amplitude of the artificial current ripple. It is a binary weighted DAC. The Differential Non-Linearity (DNL) of this DAC is less than 0.5, and the Integral Non-Linearity (INL) is less than 0.8. The schematic is shown below in figure 3.16.

4) Triangular Voltage Generator

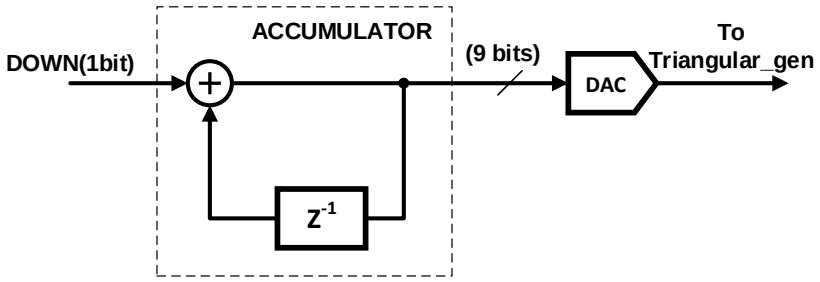


Figure 3.15: Schematic of amplitude control counter for artificial ripple current.

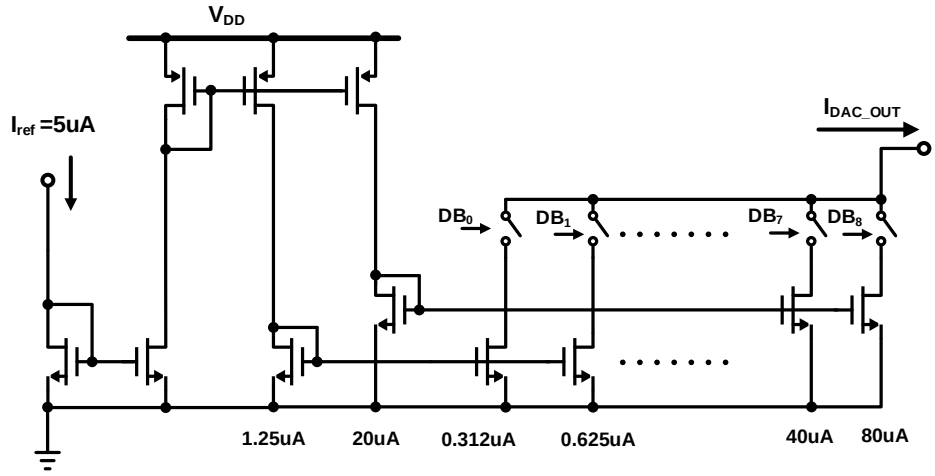


Figure 3.16: Schematic of 9-bit current steering DAC.

The triangular voltage generator and power transconductance (Gm) are forming the artificial current ripple generator. The generated triangular voltage (figure 3.17) is in opposite phase to inductor current ripple; and its amplitude is proportional to inductor current ripples amplitude.

There are four requirements for the triangular generator:

a) The magnitude of peak to peak voltage must be tuneable;

b) For steady state, V(t1)=V(t1+Ts);

c) Capacitor's charging and discharging phase must be exact opposite to inductor current;

d) Common mode or average voltage of $V_{TRI}$ should be well controlled.

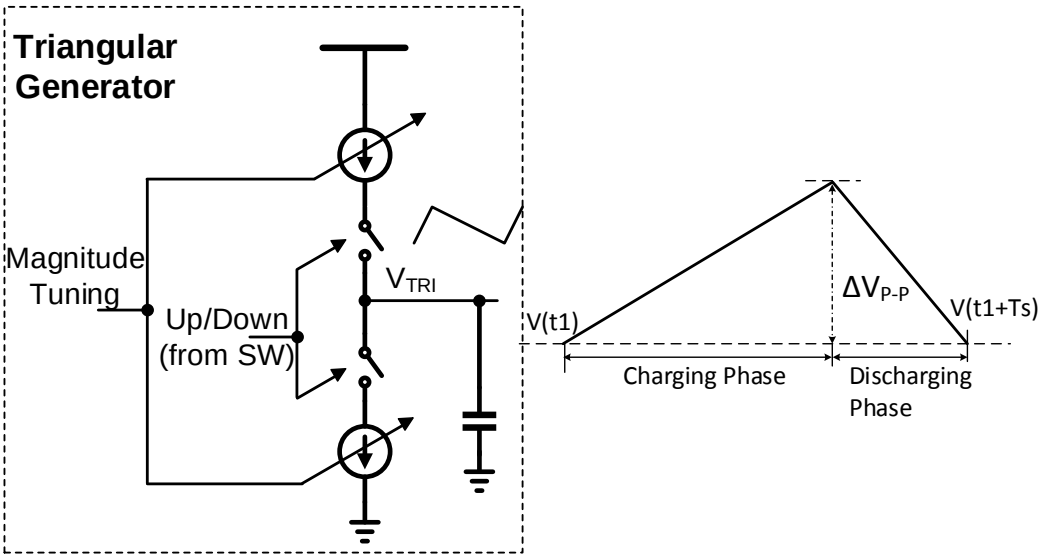


Figure 3.17: Schematic and waveform of triangular generator.

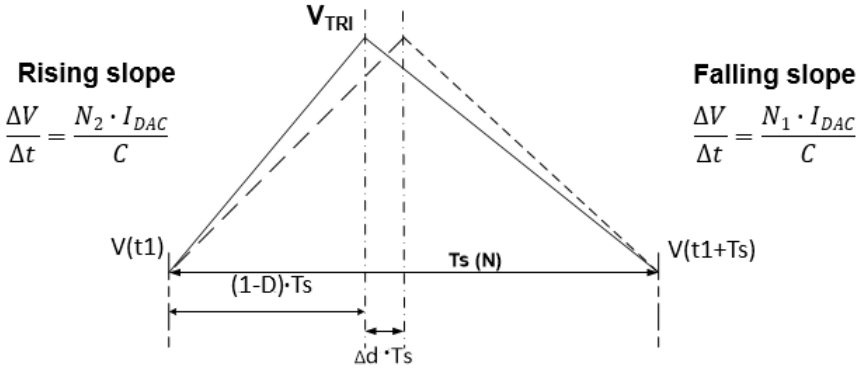


Figure 3.18: Rising and falling slope of triangular voltage.

Detailed mathematical deriviation will be presented here.

First, the 6-bit signal N1 and N2 coming from duty cycle sensing block are complimentary, N1+N2=63 (111111 in binary format), and

$$D = \frac{N1}{N1 + N2}$$

therefore,

$$\frac{N1}{N2} = \frac{D}{1 - D}$$

The duty cycle information N1 and N2 used to tune the rising and falling slope of the triangular voltage. The $I_{DAC}$ is the output of 9-bit current steering DAC.

The rising slope of triangular voltage on capacitor is

$$\frac{dV}{dt} = \frac{I_{CHARGING}}{C} = \frac{I_{DAC} \cdot N2}{C}$$

And the falling slope is

$$\frac{dV}{dt} = \frac{I_{DISCHARGING}}{C} = \frac{I_{DAC} \cdot N1}{C}$$

Next whether V(t1)=V(t1+Ts) needs to be analyzed.

$$\Delta V_{RISE} = \frac{N2 \cdot I_{DAC}}{C} \cdot D \cdot T_S = \frac{I_{DAC} \cdot T_S}{C} \cdot \frac{N1 \cdot N2}{N2 + N2}$$

$$\Delta V_{FALL} = \frac{N1 \cdot I_{DAC}}{C} \cdot (1 - D) \cdot T_S = \frac{I_{DAC} \cdot T_S}{C} \cdot \frac{N1 \cdot N2}{N2 + N2}$$

Therefore, it can be easily seen that

$$\Delta V_{FALL} = \Delta V_{RISE}$$

and V(t1)=V(t1+Ts) and steady state is guaranteed.

The detailed schematic is shown in figure 3.19. A sourcing current or sinking current connected to a capacitor generates a triangular voltage waveform. The current value is determined by both current-steering DAC and duty cycle information. Switching node SW determines whether a sourcing current or a sinking current is connected to the capacitor. If SW is high, which means inductor current is ramping up, the sinking current is connected to generate ramping down voltage; if SW is low, the sourcing current is connected to generate ramping up voltage.

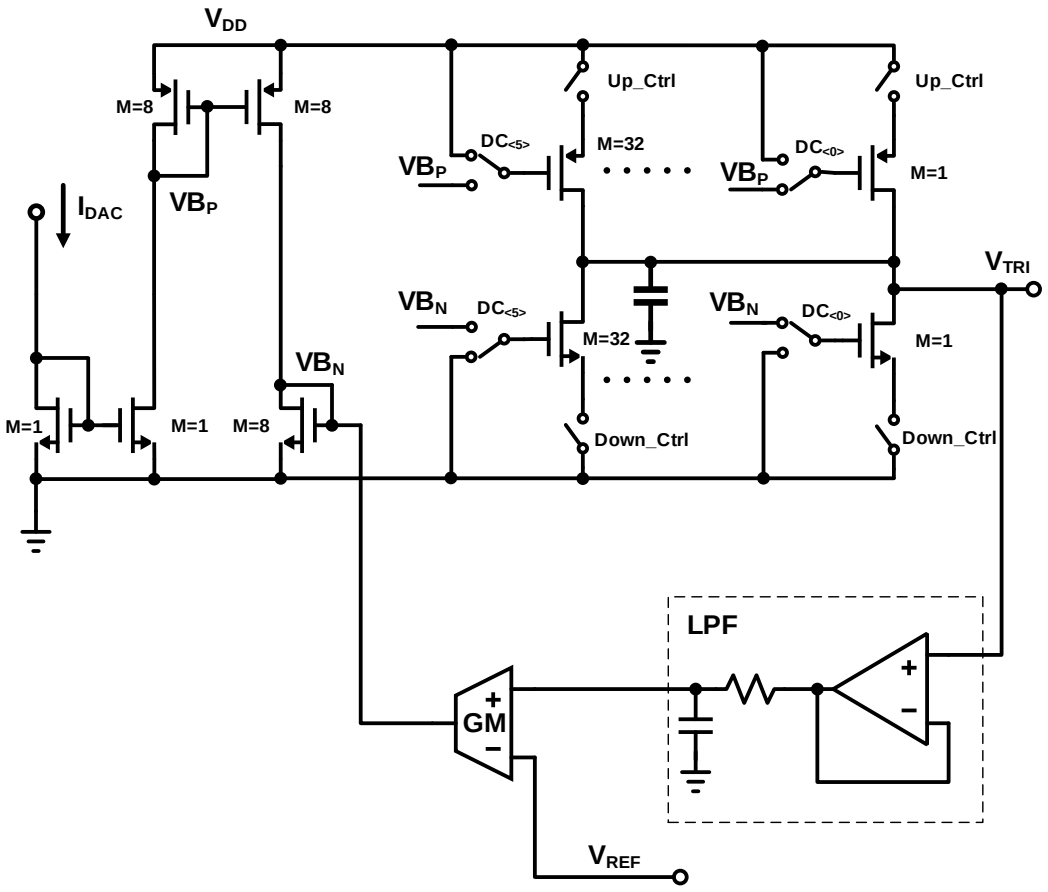


Figure 3.19: Schematic of triangular generator.

Due to current mirror mismatch, quantization error of duty cycle sensor and other non-ideality, the triangular voltage waveform will run away and gradually reach power supply or ground. If the triangular voltage is close to power supply or ground the transconductance GM block will not functions well and the cancellation scheme will fail. Therefore an auxiliary opamp, a transconductance GM and a low pass filter is used to tune the $V_{BN}$. This feedback loop forces the average value of the triangular voltage to be exactly equal to $V_{REF}$ =1V, which totally avoids triangular voltage saturating. And also the average voltage of triagular waveform is forced to satisfy input common mode range of next stage.

5) DC Blocking and Transconductance Stage

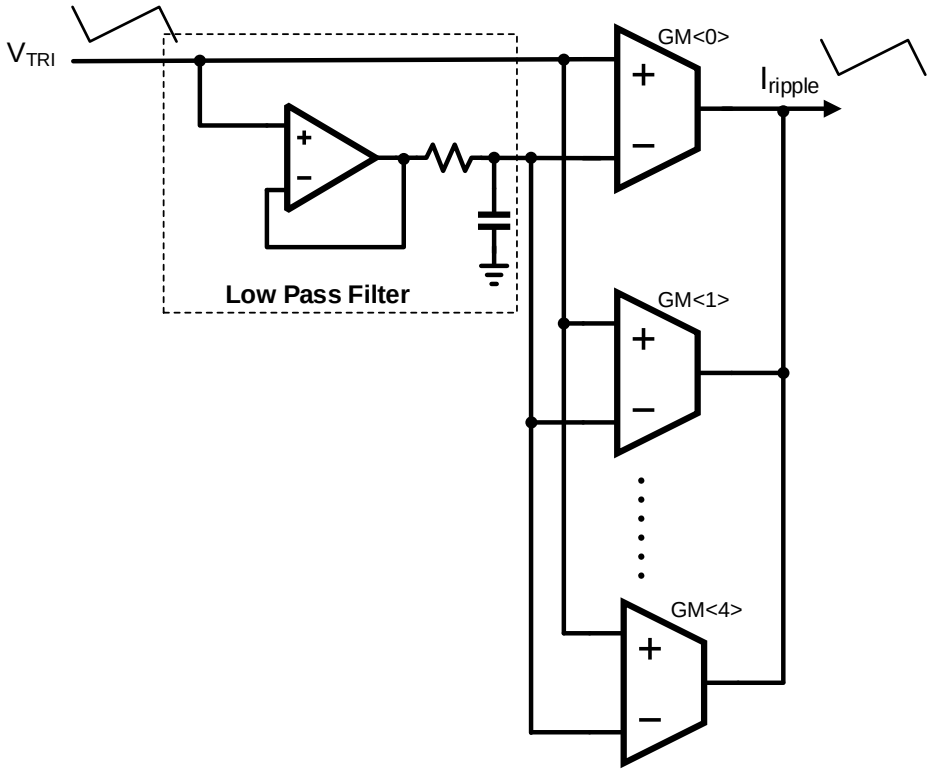


Figure 3.20: Schematic of DC blocking circuit.

Following the triangular generator is DC voltage blocking circuit and power transconductance GM stage. The GM cell has differential inputs while only the AC portion of the triangular voltage is useful. Thus a DC voltage blocking circuit is needed, which is shown in figure 3.20. The idea is simple, a large RC low pass filter is following the unity-gain buffer. A 60dB DC gain and 20MHz bandwidth folded cascode opamp is used in this buffer. Then the DC portion or very low frequency portion of the triangular voltage waveform is outputted on the big capacitor. The triangular voltage Vtri and its DC portion, $V_{TRI\_DC}$ are connected to the GM cells inputs.

The transconductance GM outputs the artificial ripple current proportional to $V_{TRI}$ voltage ripple in order to compensate the inductor current ripple [5] [13].

$$I_{RIPPLE} = gm \cdot (V_{TRI} - V_{TRI,DC})$$

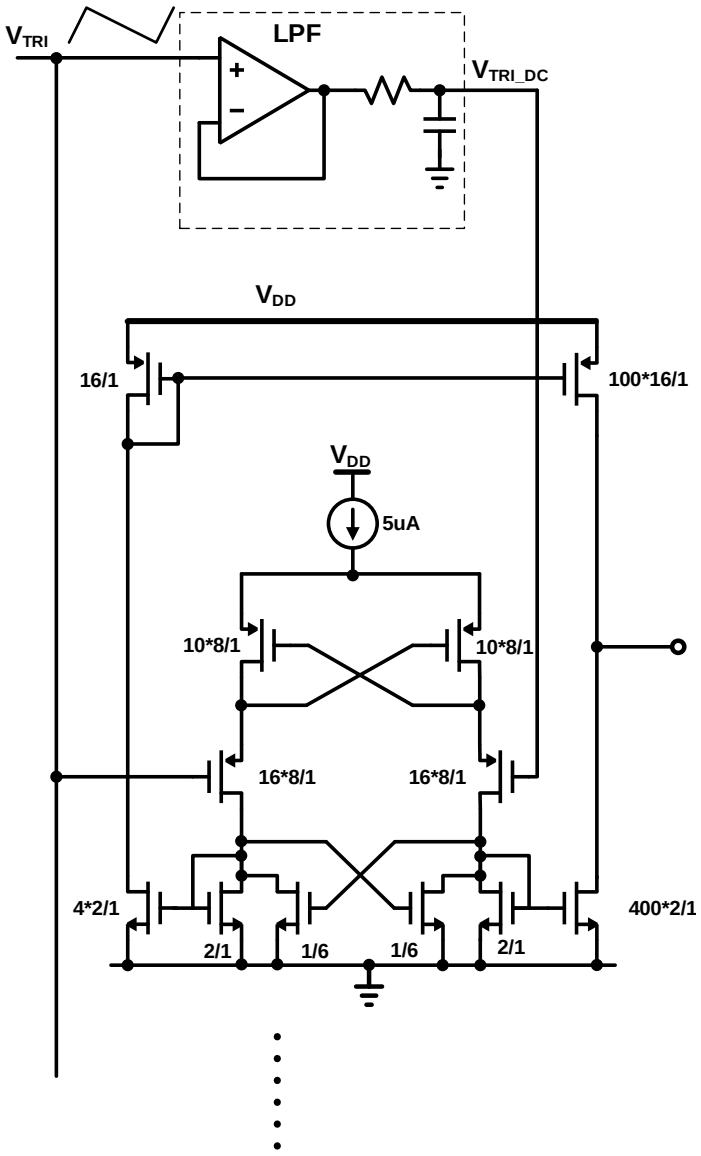


Figure 3.21: Schematic of high-power transconductance Cell.

The design difficulties of this GM stage are:

a) Large GM value to output large current. In this design, GM=4;

b) Fast response of the GM stage. In order to follow the fast-changing Vtri, the GM stage should have fast response performance.

Partial positive feedback [19] at active load of input differential pair in the GM cell helps enhance the gain and widen the bandwidth.

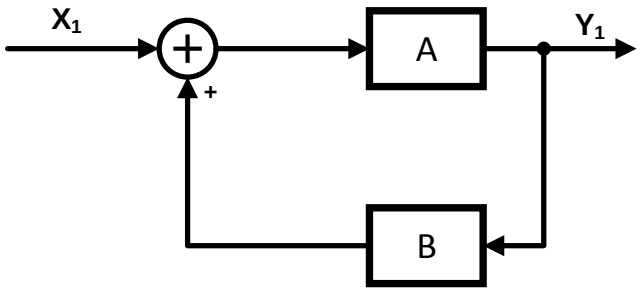


Figure 3.22: Signal flow graph of positive feedback.

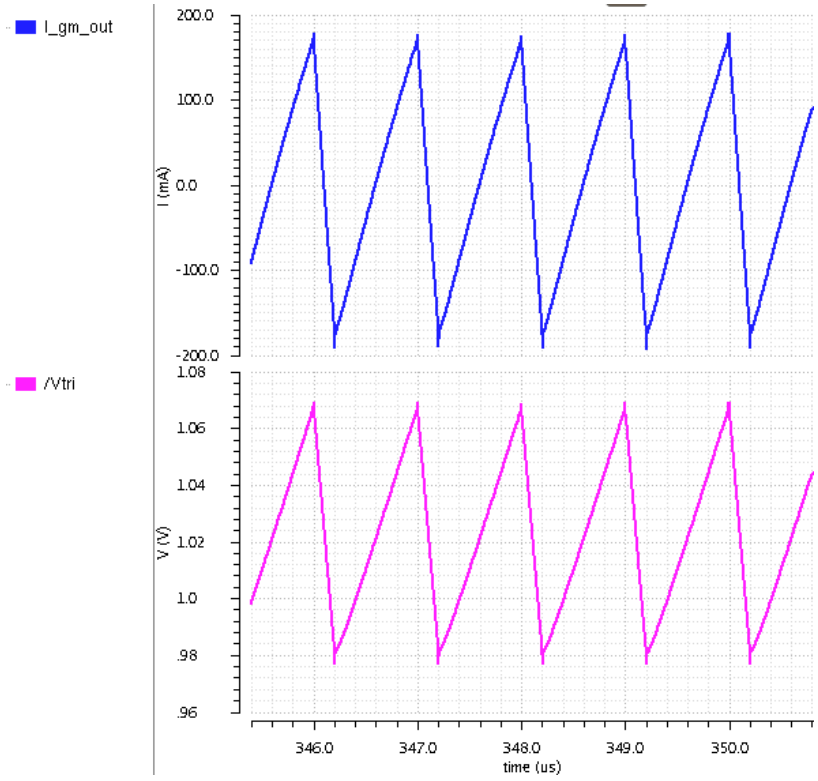


Figure 3.23: Waveform of high-power transconductance cell.

If the forward amplifier gain is A, and the feedback amplifier gain is B. The quantity $A \cdot B$ is called the loop gain. Let X1 be the input signal, Y1 be the output signal, as is shown in figure 3.22, and then the closed loop gain for an amplifier with positive feedback can be written as

$$G = \frac{Y1}{X1} = A \cdot \frac{1}{1 - A \cdot B}$$

if we set

$$0 \leq A \cdot B \leq 1$$

then the gain of the amplifier is enhanced by the factor $1/(1 - A \cdot B)$ which is greater than 1. Obviously, the value of this factor depends on the value of the loop gain $A \cdot B$, when $A \cdot B$ tends to 1, the gain factor tends to infinity, but the system tends to be unstable. On the other hand when $A \cdot B$ tends to 0, the gain factor tends to 1, i.e, no gain enhancement. Therefore a careful choice of B is important to provide maximum gain-boosting while maintaining stability. It can be seen that the positive feedback also increases bandwidth and slew rate to speed up the transient performance.

The positive feedback at source of input differential pairs help speed up the transient response too.

Furthermore, five identical gm cell are placed in parallel to boost the gm value even more.

The simulation result can be seen in figure 3.23.The first waveform is input of GM stage, with about 100mV peak to peak ripple voltage; the second waveform is output current of GM stage, with about 400mA peak to peak ripple current and its average current is very close to zero.

The effective GM value is nearly 4, which is a quite large number.

## 3.5 Phase Lock Loop

A High performance Phase Lock Loop (PLL) is needed in the system to generate accurate 64 MHz clock, whose schematic is shown in figure 3.24.

It is a common PLL [18] [14], including phase frequency detector (PFD), voltage-controlled oscillator (VCO), charge pump, frequency divider. The reference clock can be connected to SW node of Buck converter.

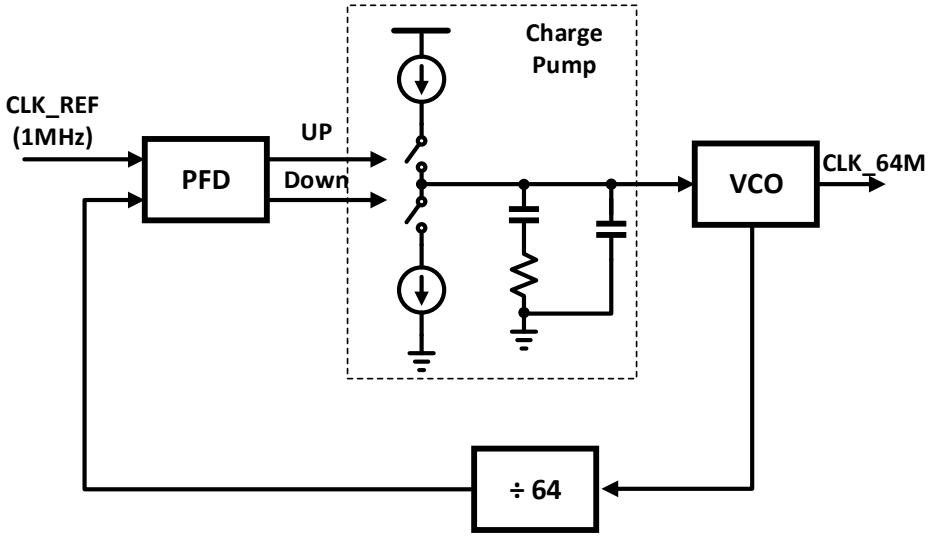


Figure 3.24: Schematic of PLL.

# Chapter 4

# SIMULATION RESULTS

## 4.1 Top Level Simulation Results

The proposed ripple canceller circuit is integrated with a buck converter together on a single chip. Two $V_{DD}$ power supplies are needed for this chip, $V_{DDP}$ and $V_{DDD}$. $V_{DDP}$ (for example, 5V, or 3V) is for buck converter and high-power GM stage in canceller; the other one $V_{DDD}$ (for example, 1.8V) is used for all parts except above two.

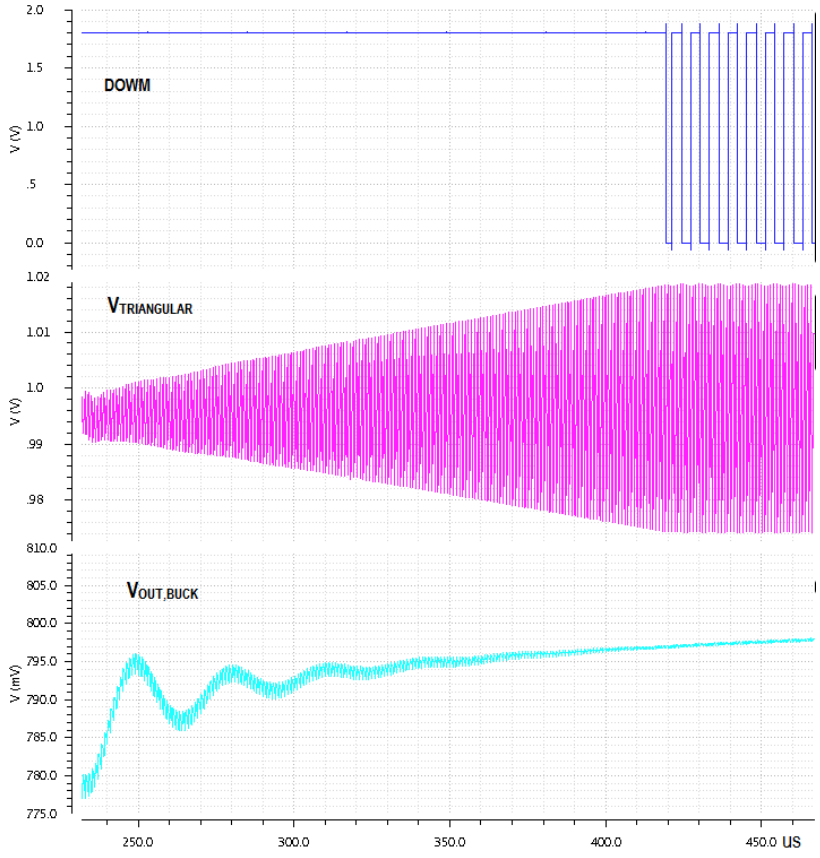


Figure 4.1: Top level simulation results.

In the top level simulation test bench, $V_{DDP}$, the power supply for buck converter, is

connected to 5V. $V_{OUT,BUCK}$ is set to 1V, and the load current of buck convertr is 1A.

The top level simulation result is shown below in figure 4.1.

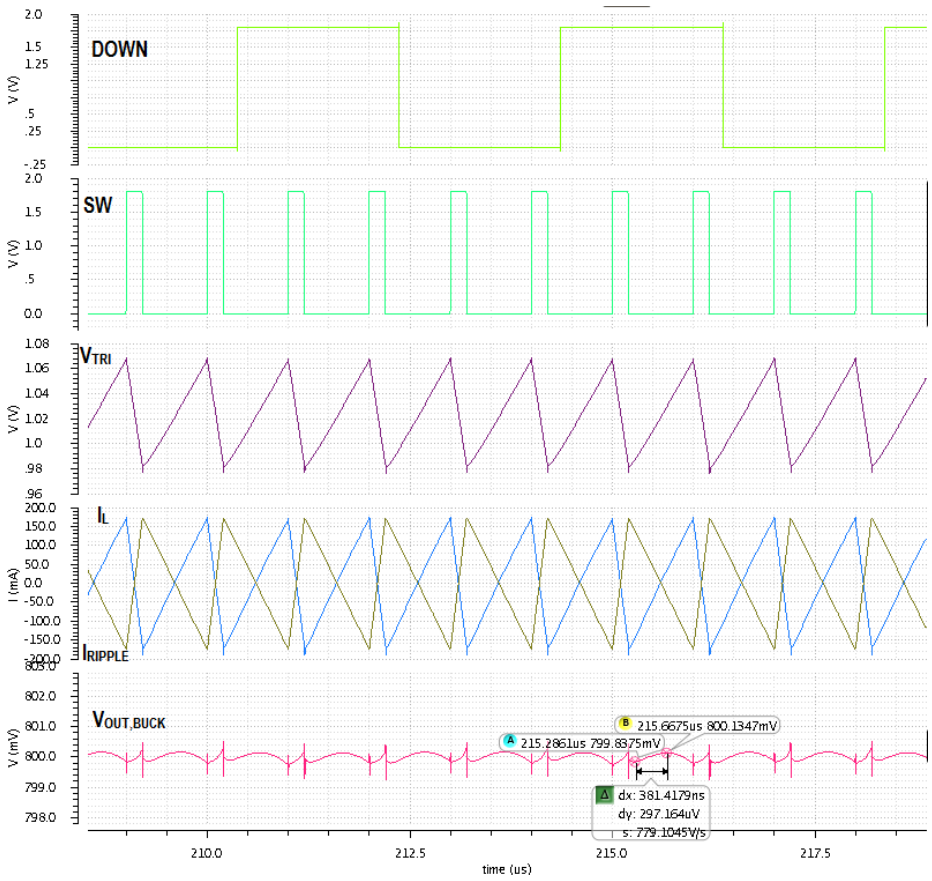


Figure 4.2: Zoom-in view of top level simulation results.

From the transient simulation result, it can be seen that before ripple cancellation circuit is enabled, the output voltage ripple of Buck converter is about 3mV. After ripple cancellation circuit is enabled, the swing of triangular voltage waveform becomes larger and larger. When the cancellation circuit settles down, the ripple voltage on Buck output have been reduced to less than 300uV, i.e. about 10X reduction. Also, from the zoom in view, figure 4.2, it can be seen that the generated ripple current has the same amplitude as inductor current ripple but exact opposite phase.

A DFT analysis is done based on the transient simulation result. After DFT analysis,

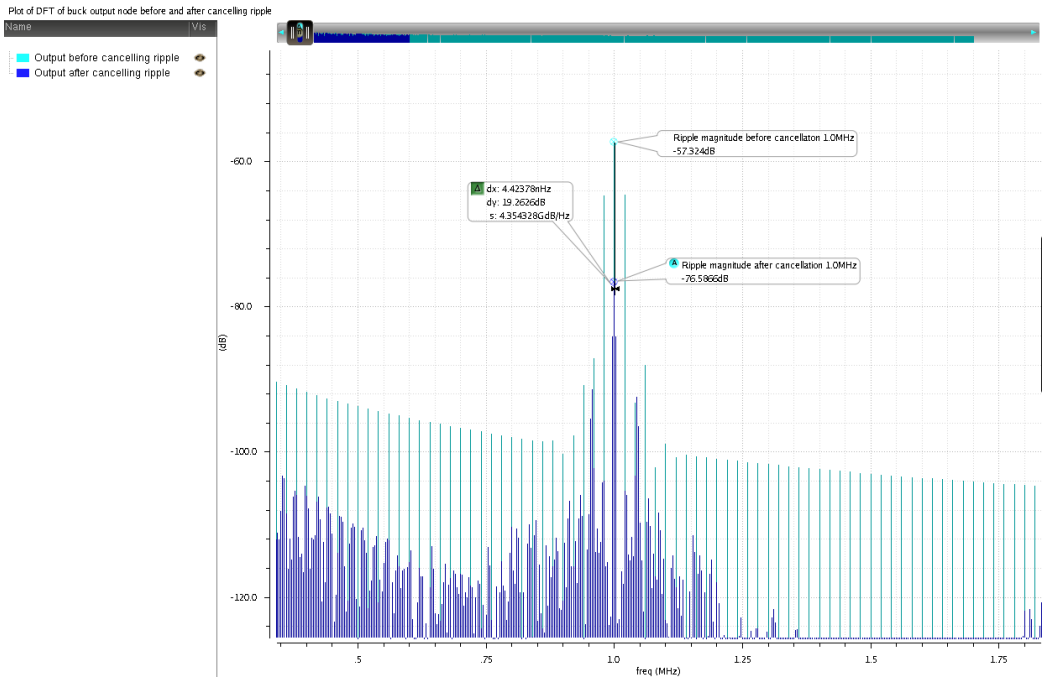


Figure 4.3: DFT analysis result of top level simulation.

the power spectrum of buck output can be seen. From the result in figure 4.3, before the canceller enabled, the power at 1 MHz is -57dB; after the canceller settled, the power at 1MHz is -76dB, which is about 19.3dB ripple rejection. Also the noise floor gets reduced obviously after enabling the canceller.

## 4.2 Power Comparison Summary

Power dissipation analysis based on the transient simulation result is needed. The derivation of power dissipation is covered here to compare ripple canceller technique with LDO.

For LDO total power loss,

$$P_{TOTAL} = I_Q \cdot V_{DD} + I_{OUT} \cdot V_{DROPOUT}$$

In the equation, the first part is the quiescent power loss, the second part is the dropout

power loss. To have high PSR, the dropout voltage is usually higher than 1V, which makes the dropout power loss quite huge.

For the total power loss of ripple canceller.

$$P_{TOTAL} = I_Q \cdot V_{DD} + P_{RMS,TRI}$$

The first part in the equation is the quiescent power loss of the canceller. The second part is RMS TRI current power loss from GM stage, as is in figure 4.4, which can be described in the next equation,

$$P_{RMS,TRI} = P_{POS} + P_{NEG} - P_{DELIVERED}$$

where,

$$P_{POS} = (V_{DD} - V_{OUT}) \cdot I_{RMS,POS}$$

$$P_{NEG} = V_{OUT} \cdot I_{RMS,NEG}$$

$$P_{DELIVERED} = V_{OUT} \cdot I_{RMS,OUT}$$

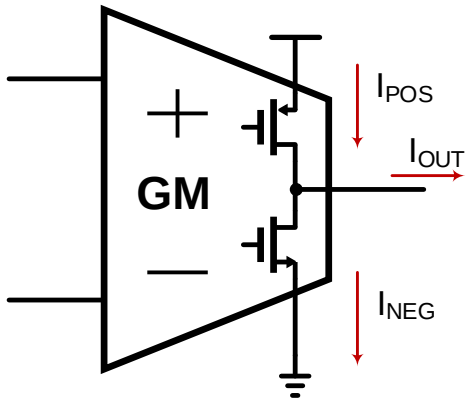


Figure 4.4: Schematic for canceller's GM power loss calculation.

The calculation result is shown in table 4.1. LP38500 is TIs 1A output, Flexcap low-dropout linear regulator. It can be seen that the proposed ripple cancellation technique has much less power dissipation.

Table 4.1: Power Dissipation Comparison Summary

| | LP38500 | Ripple Canceller |
|---|---|---|
| $I_{OUT,MAX}$ (A) | 1 | 1 |
| $V_{OUT}$ (V) | 0.8 | 0.8 |
| $I_{Q,TYP}$ (mA) | 5 | 1.3 |
| $V_{DROPOUT}$ (V) | 1.5 | |
| Dropout Power Loss (mW) | 1500 | |
| Quiescent Power Loss (mW) | 12 | 2 |
| Triangular Power Loss (mW) | | 908 |
| Total Power Dissipation (mW) | 1512 | 910 |

## 4.3 IC Layout

The ripple cancellation together with a buck converter is fabricated in 250nm CMOS technology with 4 metal layers. This PDK has 1.8V and 5V transistors required for the system design.

Complete system layout is present in figure 4.5. Dimension of IC is $3.17mm$ X $3.05mm$ i.e total area is $9.6mm^2$. And the area of the proposed canceller is only $2.3mm^2$.

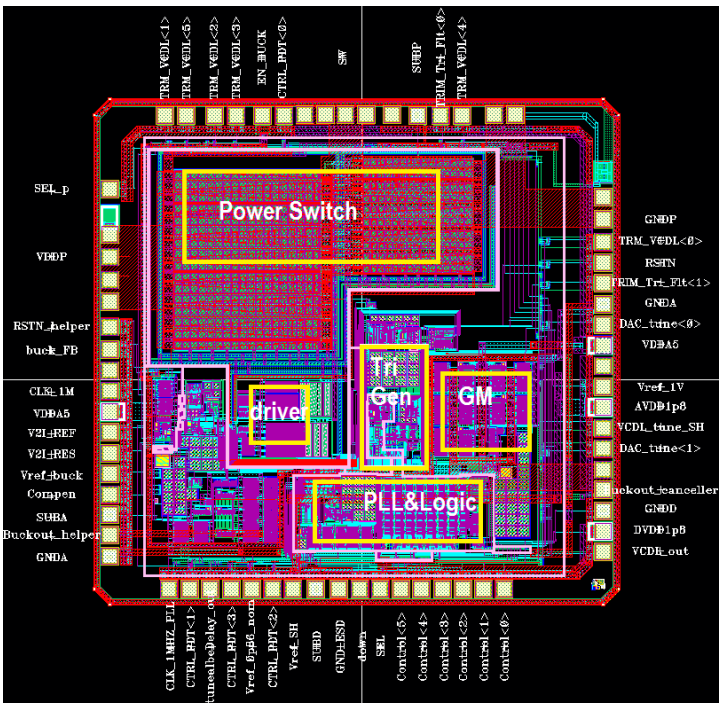


Figure 4.5: IC Layout of the System

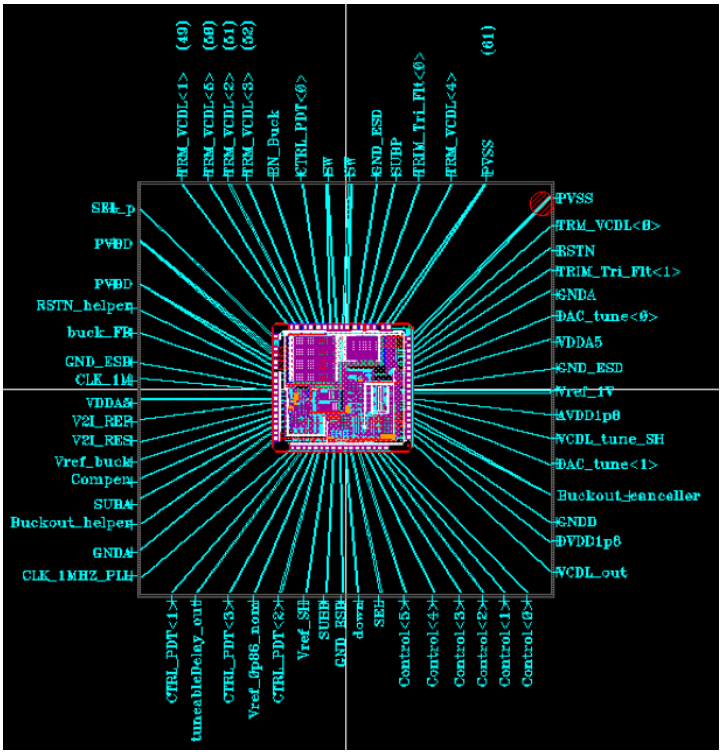

Figure 4.6: Bonding Diagram

# Chapter 5

# CONCLUSION AND FUTURE WORK

To reject ripple voltage on buck converter output, a mixed signal adaptive ripple cancellation technique for buck converter is developed. The idea is build an adaptive artificial AC ripple current that has the same amplitude as inductor current ripple but exact opposite phase.

The power dissipation of proposed canceller is much smaller than any scheme with LDO. Because the DC output currnet is flowing through pass device of a LDO, but only AC current is flowing through the transconductance stage of ripple canceller.

There are four main parts in the ripple canceller:

1) Duty cycle sensing;

2) Artificial ripple amplitude control;

3) High-power transconductance stage;

4) A 64 MHz phase lock loop.

The duty cycle sensing block is functioning as a TDC (Time to Digital Converter) to convert buck converter's on time interval into a 6-bit duty cycle information code.

The peak and valley value of buck output voltage are sampled and fed into the input of a high-speed comparator. The comparator outputs a 1-bit signal which indicates whether the peak value is much higher than the valley value. This 1-bit signal is fed into the amplitude control counter or digital low pass filter, and controls a 9-bit current-steering DAC. The output current of the DAC together with 6-bit duty cycle information determines a triangular voltage generator's peak to peak amplitude and phase. Followed by DC blocking circuit, the triangular voltage waveform is fed into a high-power transconductance stage. The artificial ripple current comes out of the transconductance stage.

From the top level simulation results, it can be seen that there is 20dB ripple rejection on the buck converter's output at switching frequency. and the power dissipation of this ripple canceller is much smaller than the solution with LDO.

The ripple canceller together with a buck converter is fabricated in 250nm CMOS technology with 4 metal layers. This PDK has 1.8V and 5V transistors required for the system design. The dimension of IC is $3.17mmX3.05mm$, i.e total area is $9.6mm^2$. And the area of the proposed canceller is only $2.3mm^2$.

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